PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
H01L 23/48, 21/44

A1

(11) International Publication Number: WO 99/57762

(43) International Publication Date: 11 November 1999 (11.11.99)

(21) International Application Number: PCT/SG99/00035

(22) International Filing Date: 30 April 1999 (30.04.99)

(30) Priority Data:
9800994-7 2 May 1998 (02.05.98) SG

(71) Applicant: ERISTON INVESTMENT PTE LTD. [SG/SG]; 9 Battery Road #08-03, Straits Trading Building, Singapore 049910 (SG).

(72) Inventor: LIN, Charles, W., C.; 55 Cairnhill Road #21-04, Cairnhill Plaza, Singapore 229666 (SG).

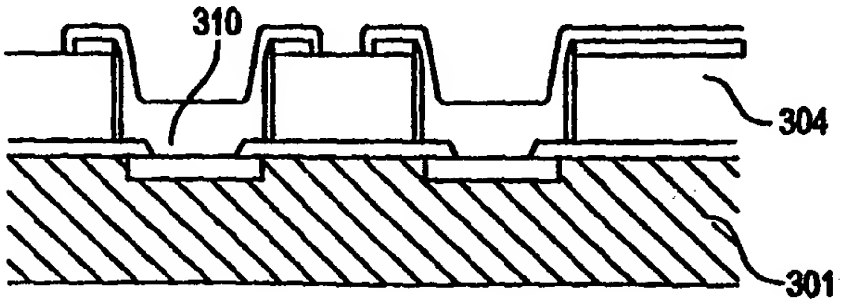
(74) Agent: LAWRENCE Y. D. HO & ASSOCIATES; 30 Bideford Road #07-01, Thongsia Building, Singapore 229922 (SG).

(81) Designated States: CN, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: FLIP CHIP ASSEMBLY WITH VIA INTERCONNECTION

(57) Abstract



A flip chip assembly, and methods of forming the same, including a single layer or multilayer substrate in which via holes serve as connections between a semiconductor chip and the substrate. The assembling steps comprise attaching an integrated circuit chip to a rigid or flexible dielectric substrate having a plurality of via holes for connecting respective traces in the substrate with respective input/output terminal pads of the integrated circuit chip. The via holes are aligned and placed on top of the pads so that these pads can be totally or partially exposed through the opposite side of the substrate. Electrically conductive material is subsequently deposited in the via holes as well as on the surface of the pads to provide electrical connections between the integrated circuit chip and the traces of the dielectric circuitry. After via holes are connected, means in bring in chip and substrate attachment can be removed or left as an integral part of the assembly since these connections can also provide mechanical support. The contacting materials include electroless plated metals, electrochemical plated metals, solders, epoxy and conductive polymers.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece			TR	Turkey
BG	Bulgaria	HU	Hungary	ML	Mali	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MN	Mongolia	UA	Ukraine
BR	Brazil	IL	Israel	MR	Mauritania	UG	Uganda
BY	Belarus	IS	Iceland	MW	Malawi	US	United States of America
CA	Canada	IT	Italy	MX	Mexico	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NE	Niger	VN	Viet Nam
CG	Congo	KE	Kenya	NL	Netherlands	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NO	Norway	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	NZ	New Zealand		
CM	Cameroon			PL	Poland		
CN	China	KR	Republic of Korea	PT	Portugal		
CU	Cuba	KZ	Kazakstan	RO	Romania		
CZ	Czech Republic	LC	Saint Lucia	RU	Russian Federation		
DE	Germany	LI	Liechtenstein	SD	Sudan		
DK	Denmark	LK	Sri Lanka	SE	Sweden		
EE	Estonia	LR	Liberia	SG	Singapore		

FLIP CHIP ASSEMBLY WITH VIA INTERCONNECTION

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to integrated circuits assembly, and in particular, to the electrical connection of integrated circuits to substrate circuitry, printed circuit board, and interconnect components. Most specifically, the invention relates to the assembling methods and apparatus of flip chip assembly which includes a single or multi-layered substrate in which via holes are electrically and mechanically connected to the input/output terminal pads of the integrated circuits through direct metallization.

2. Related Art

Recent developments of semiconductor packaging suggest an increasingly critical role of the technology. New demands are coming from requirements for more leads per chip and hence smaller input/output terminal pitch, shrinking die and package footprint, higher operational frequency that generate more heat, thus requiring advanced heat dissipation designs. In addition to these demands, the more stringent

electrical requirements must not be compromised by the packaging. All of these considerations must be met and, as usual, placed in addition to the cost that packaging adds to the semiconductor-manufacturing food chain.

Conventionally, there are three predominant chip-level connection technologies in use for integrated circuits, namely wire bonding, tape automated bonding (TAB) and flip chip (FC) to electrically or mechanically connect integrated circuits to leadframe or substrate circuitry. Wire bonding has been by far the most broadly applied technique in the semiconductor industry because of its maturity and cost effectiveness. However, this process can be performed only one at a time between semiconductor chip's bonding pads and the appropriate interconnect points. Furthermore, because of the ever increasing operational frequency of the device, the length of the interconnects needs to be shorter to minimize inductive noise in power and ground, and also cross-talk between the signal leads. An example of such a method is disclosed in U.S. Pat. No. 5,397,921 to Karnezos et al.

Flip chip technology is defined as mounting of an unpackaged semiconductor chip with the active side facing down to a interconnect substrate through some kind of contact anchors such as solder, gold or organic conductive adhesive bumps. The major advantage of flip chip technology is the short interconnects which, therefore, can handle high speed or high frequency signals. There are essentially no parasitic elements such as inductance. Not only is the signal propagation delay slashed, but much of the waveform distortion is also eliminated. Flip Chip also allows an

area array interconnecting layout that provides more I/O than a perimeter interconnect with the same die size. Furthermore, it requires minimal mounting area and weight which results in overall cost saving since no extra packaging and less circuit board space is used. An example of such a method is disclosed in U.S. Pat. No. 5,261,593 to Casson et al.

FIG. 1 is a schematic cross-sectional view of a prior art flip chip assembly in which an integrated circuit chip 101 is attached to a substrate 102 through electrically conductive bumps 103. These bumps 103 make electrical connection between selected one of bond pads 104 formed on the chip and specific one of the conductive traces 105 formed on the surface of the substrate 102. These traces 105 will further extend to the other side of the substrate through via holes 107 that are formed within the substrate 102. In the structure of dielectric substrate, via hole is a method of connecting either two or multiple layers of circuitry in a substrate. It can link both sides of the finished substrate, whereas blind via link one side to one inner layer or multiple layers and buried via links internal layers without being visible on the surface of the board. These vias are typically metallized on the sidewall with copper by electroless and electroplating. Underfilled material 106 is typically applied between integrated circuit chip 101 and substrate 102 in order to release the stress due to thermal characteristic mismatch of the integrated chip 101 and substrate 102. Conductive traces 105 formed on the top of the substrate extend from the holes and vias to specific contacting pads or balls 108 and therefore connect to the external circuitry.

While flip chip technology has tremendous advantages over wire bonding, its cost and technical limitations are significant. First of all, flip chip technology must confront the challenge of forming protruded contact anchors or bumps to serve as electrical connections between integrated circuit chip and substrate circuitry. A variety of bumping processes have therefore been developed. These include a vacuum deposition of intermediate under-bump layer system which serves as adhesive and diffusion barrier. This barrier layer is composed of a film stack which can be in the structure of chromium/copper/gold. Bumping materials such as solder are subsequently deposited onto this intermediate layer through evaporation, sputtering, electroplating, solder jetting or paste printing methods followed by a reflow step to form the solder contacts.

Techniques for fabricating the intermediate under-bump barrier layer as well as bump material utilizing electroless plating are also known. In these attempts, as shown in FIG 2, the input/output terminal pads 201 of the integrated chip 200 are firstly activated by a catalytic solution which will selectively activate the pad material through chemical reactions and form a thin layer of catalyst 202. This thin layer of catalyst 202 is typically composed of zinc or palladium element. When electroless plating is executed thereafter, material such as nickel, gold, palladium or their alloys can be selectively initiated and continuously deposited on the pad to form the bumps 203. In the above-described electroless plating process, hypophosphate or boron hydride are commonly used as reducing agent in the nickel plating solution. This electroless plated bump not only provide the

protruding contact anchor but also served as the diffusion barrier and sealing purposes. Contacting material such as solder, conductive adhesive or polymer is subsequently applied onto these bumps by techniques such as solder dipping, solder jetting, evaporation, screen printing or dispensing. An example of such a method is described in the U.S. Pat. No. 5,583,073, Lin et al.

Although electroless technique provides an economical, simple and effective method for under bump barrier layer, contacting material such as solder or adhesive is still required for assembling. Solder dipping or screen printing of solder paste onto these bumps has been explored but with very limited success due to solder bridging control and non-uniform deposition of solder on the metal bump. This process can be very troublesome; it suffers from poor process control as the input/output terminal pad space is ever getting smaller and smaller. Additional problems have been encountered with the tin/lead solder systems due to its increase in electrical resistance over time. Moreover, the solder contacts are easily fatigued in thermo-mechanical stressing.

Organic contacts which utilize conductive adhesive to replace solder joint is also described in U.S. Pat. No. 5,627,405, Chillara. Generally speaking, the conductive adhesive which is made by adding conductive fillers to polymer binders, holds a number of technical advantages over soldering such as environmental compatibility, lower-temperature processing capability, and fine pitch and simplified processes. However, this type of adhesives does not normally form the metallurgical interface in the

classical sense. The basic electrical pathway is through conductive particles of the adhesives that are in contact with one another and reach out to the two contact surfaces of the components. Under certain environments, this interconnect system may cause problems because the penetration of moisture through polymer may induce corrosion and oxidation of the conducting metal particles which results in unstable electrical contacts. Furthermore, failure of the joints can also occur due to degradation of the polymer matrix as well as degradation of the metal parts. Since the electrical and mechanical performance is independent of each other, a good mechanical performance is no assurance of its electrical integrity.

In view of the limitations in the currently available integrated circuits assembling methods, a high-performance, reliable and economical method which interconnects integrated circuits to the external circuitry would be greatly desirable.

SUMMARY OF THE INVENTION

According to the invention, a flip chip assembly is provided to address high density, low cost and high performance requirements of electronics products. It involves the direct interconnection of integrated circuit to a substrate circuitry through direct metallization of via holes and bond pads without the need of bumps, wire bonds, or other media.

To achieve the foregoing and in accordance with the invention, the assembly includes a rigid or flexible dielectric substrate having a plurality of

electrically conductive circuitry, one or more integrated circuit chips having a plurality of input/output terminal pads, and a plurality of via holes formed in the dielectric substrate for electrically connecting respective traces of the substrate with respective pads of the integrated circuit chip. The surface of the integrated circuit chip and the dielectric substrate may be arranged in substantially mutually parallel planes. The orientation of the contact is in such a manner that the via holes in the dielectric substrate are aligned on the top of the pads of the integrated circuit chip so that these pads can be totally or partially exposed through the opposite side of the substrate. After the alignment, the connecting step may include attaching the integrated circuit chip to the dielectric substrate through mechanical or chemical techniques thus form an assembly. Electrically conductive material is subsequently deposited in the via holes as well as on the surface of the input/output pads of the integrated circuits to provide electrical and mechanical connections between the chips and the traces of the dielectric circuitry. After via holes is connected to the terminal pads, the mechanical and chemical means in bring in chip and substrate attachment can be removed or left as an integral part of the assembly since these connections can also provide mechanical support.

In a method aspect of the invention, the connection method is by electroless plating. The electroless plating will initiate and continuously deposit electrical conductive material such as copper, nickel, palladium, gold and their alloys on the via hole wall as well as input/output terminal pads of the integrated chip. As the plating process continues, the metallic

surface of the via holes sidewall and terminal pads will extend out and contact each other and finally join together and become an integrated part. These simultaneously electrolessly plated joints will provide an effective means for electrical and mechanical connections between the integrated chip and the dielectric circuitry.

In another method aspect of the invention, the connection method may take the form of electrochemical plating. In this method, metallized via holes in the dielectric substrate are electrically connected to the external power source and serve as one electrode for plating. This plating process can be carried out on the sidewall of via holes as well as other areas where electricity can be reached and chemical solution is exposed to. In the initial stage, the terminal pads of the integrated circuit chip do not receive electroplating due to no electrical contact. However, as the via hole sidewall plating process continues, the metallizing surface will extend out and finally contact and provide electricity to the terminal pads and subsequently initiate electroplating on them. These simultaneously electroplating parts will then join together and provide an effective means for electrical and mechanical connections between the chip and the dielectric circuitry.

According to a further aspect of the invention, the connection method may take the form of solder paste, liquid solder or solder particle, which are reflowable and bondable to the integrated circuit chip terminals and via hole walls after application of heat or certain form of energy such as laser or infrared light. In this method, solder paste or solder particles will be filled into the vias through selective printing, jetting or ball placement techniques.

As the external energy such as heat or laser applies to the filling material, the original form of the material will melt and change its shape, enlarge the contacting areas, adhere to the wettable surfaces thus providing an effective means for electrical and mechanical contacts between pre-metallized via hole wall and input/output terminals of the integrated circuit chips. In some embodiments, these input/output terminals should be pre-treated or coated with a thin protective layer if the material has a tendency to be chemical attacked such as corrosion or dissolution through some form of reactions by the joint material such as solder.

According to the invention, via holes of the substrate circuitry can be formed by various techniques including mechanical drilling, punching, plasma etching or laser drilling. They are formed in the substrate at locations where electrical circuitry on one side of the substrate can be connected to the opposite side of the surface on which the semiconductor chip or chips are mounted and their input/output terminal pads can be exposed through these holes.

According to the invention, dielectric layers of the rigid substrate can be either organic or inorganic material. Organic type substrate is preferable for the purpose of lower cost, superior dielectric property whereas inorganic type of substrate is preferable when high thermal dissipation and matched coefficient of expansion are desired.

If the finished product is, for instance, a ball grid array, solder balls can be formed on the pads on the opposite side of the circuitry. This finished package can be connected to a printed circuit board by reflowing the solder

ball to form an attachment to the traces on the surface of the printed circuit board.

In summary, using via hole direct connection of integrated circuit chip and dielectric substrate circuitry instead of anchoring solder or conductive adhesive bump allows high reliability, low profile, and high performance assembly to be achieved. In particular, a small via hole which can be formed by laser or other techniques allows very fine pitch terminal pad to be interconnected, can significantly enhance the capability of packaging future high I/O semiconductor chips.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 (prior art) is a diagrammatic cross-sectional view of a conventional flip chip package with solder bumps

FIG. 2 (prior art) is a diagrammatic cross-sectional view of a prior art showing a electroless plated nickel bump structure

FIGS. 3A to 3D are diagrammatic cross-sectional views showing the steps involved in the manufacturing of an integrated circuits assembly by electroless plating according to the present invention.

FIGS. 4A to 4E are diagrammatic cross-sectional views showing the steps involved in the manufacturing of an integrated circuit assembly by electroless via fill according to another embodiment of the invention.

FIGS. 5A to 5E are diagrammatic cross-sectional views showing the steps involved in the manufacturing of an integrated circuit assembly by electroplating according to another embodiment of the invention.

FIGS. 6A to 6D are diagrammatic cross-sectional views showing the steps involved in the manufacturing of an integrated circuit assembly by solder via fill according to another embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention will be illustrated further by the following examples. These examples are meant to illustrate and not to limit the invention, the scope of which is defined solely by the appended claims.

EXAMPLE 1

FIGS. 3A through 3D illustrate a process for producing an embodiment of the flip chip assembly according to the present invention. Referring initially to FIG 3A, an integrated circuit chip 301 in which various types of transistor, wiring and the like were formed (not shown) having a plurality of input/output terminal pads 302 exposed. These pads 302 were firstly cleaned by dipping the integrated circuitry chip 301 in a phosphoric acid solution at room temperature with an immersion time of 10 minutes to remove the surface oxide film. This chip was next dipped in a diluted catalytic solution Enthone "Alumon EN" (trademark) at 25 degree C for 20

s conds to form a thin zinc film 303 on the surface of the aluminum alloy terminals 302, followed by a thorough distillated water rinse to ensure there is no residue left on the surface of integrated circuitry chip.

FIG. 3B shows a double-sided or multi-layer dielectric substrate 304 having a plurality of electrically conductive circuitry traces 305 attached to the integrated circuit chip. The traces 305 on one surface of the substrate 304 extend to a plurality of via holes 306 of the dielectric substrate 304. The metallic film 307 on the sidewall of the via holes was formed by conventional techniques including electroless plating, sputtering or evaporation or a combination of these techniques. These holes 306 are arranged in such a manner that the terminal pads 302 of the integrated circuit chip 301 can be totally or partially exposed when integrated circuit chip 301 is mounted on the substrate 304. These holes 306 are to serve as electrically connecting channels for respective traces 305 on the top surface of the substrate 304 with respective terminal pads 302 of the integrated circuit chips 301. The metallic film on the sidewall of via holes was activated by immersing in the palladium chloride solution (0.05 M) for readily initiating electroless plating.

Now referring to FIG. 3C, after integrated chip 301 is securely attached to the substrate 304, the integrated chip assembly is immersed in the electroless plating solution Shipley "NIPOSIT 468" (trademark) at 65 degree C. The electroless plating will initiate and continuously deposit a thin layer of nickel film 308 containing phosphorous (to be referred to as a nickel film hereafter) on the pre-activated metal film 307 and nickel film 309 on the

input/output terminal pads 302 of the integrated circuits chips 301. As the plating process continuous,

FIG 3D shows the metallic surface of the via hole wall and input/output terminals finally contact and join together become an integrated part 310. These simultaneously plated joints will then provide an effective means for electrical and mechanical connections between the input/output terminals and the traces of the dielectric circuitry.

Though only one integrated circuit chip 301 is shown in the figure, it is to be understood that additional integrated circuit chips, as well as passive components such as resistors or capacitors, can also be mounted on substrate 304.

EXAMPLE 2

FIGS. 4A through 4E illustrate a process for producing another embodiment of the flip chip assembly according to the present invention. Referring now to FIG 4A, an integrated circuit chip 401 similar to that in example 1 was cleaned in an alkaline solution containing 0.02 M sodium hydroxide at room temperature (25 degree C) with immersion time of 1 minute. This chip 401 was next dipped in a catalytic solution Shipley "DURAPREP 40" (trademark) at 25 degree C with immersion time of 2 minute to form an activation layer 403 on the surface of the terminal pads 402. After a thorough rinse in distilled water, the integrated circuitry chip was immersed in a Shipley "NIPOSIT 468" (trademark) electroless plating bath

for 2 minutes, at 65 degree C. A thin layer of nickel film 404 containing phosphorous (to be referred to as a nickel film hereafter) was precipitated on and around the terminals 402.

FIG 4B shows a dielectric substrate 405 having a sheet of copper 406 on the top of the surface and covered by a layer of insulating film 407. A plurality of through holes 408 are drilled and arranged in such a manner that the input/output terminal pads 402 of the integrated circuit chip 401 can be totally or partially exposed when integrated circuit chip 401 is mounted on the substrate 405. There is no activation layer or metallized film on the hole wall.

FIG. 4C shows the integrated circuit chip 401 securely attached to the substrate 405, the integrated circuitry chip assembly is then immersed in the electroless plating solution Shipley "NIPOSIT 468" (trademark) at 65 degree C. The electroless plating will initiate and continuously deposit nickel pillar 409 on the top of the pre-deposited nickel film 404 (shown in phantom lines) of the integrated circuit chips 401.

FIG. 4D shows that the plated nickel 409 has reached the dielectric edge of the hole 408 and finally contact with the top layer of copper sheet 406. The insulating film 407 was stripped off after the nickel via-fill reached the copper sheet. These plated joints will then provide an effective means for electrical and mechanical connections between the input/output terminals and the top surface of the dielectric circuitry.

FIG. 4E shows a plurality of copper circuitry traces 410 formed on the surface of the substrate by conventional etching techniques. These traces

410 extend from a plurality of electroless nickel-filled holes 408 of the dielectric substrate 405 and serve as electrically connecting channels with respective input/output terminal pad 402 to the external circuitry.

EXAMPLE 3

FIGS. 5A through 5E illustrate a process for producing another embodiment of the flip chip assembly according to the present invention. Referring now to FIG 5A, an integrated circuit chip 501 similar to that in example 1 was cleaned in an alkaline solution containing 0.05 M phosphoric acid at room temperature (25 degree C) with immersion time of 1 minute. The chip was then thoroughly rinsed in distillated water to ensure there is no residue left on the surface of integrated circuitry chip. A multi-layered thin film 503 having the structure of chromium (500 A)/copper (700A)/gold (1000 A), respectively, was selectively deposited on the terminal pads 502 to serve as barrier and adhesive layer.

FIG 5B shows a dielectric substrate 504 having a sheet of copper 505 on the top of the surface and covered by a layer of insulating film 506. A plurality of via holes 507 having a thin copper film 508 on the sidewalls is arranged in such a manner that the input/output terminal pads 502 of the integrated circuit chip 501 can be totally or partially exposed when it is mounted on the substrate 505.

FIG. 5C show the assembly immersed in the copper plating solution Sel-Rex "CUBATH M" (trademark) at 25 degree C. An electric power source

is connected to the copper 505 on the top surface of the dielectric substrate. Electroplating reaction will initiate and continuously deposit copper 509 on the sidewall of the via holes. As the plating process proceeds, the sidewall copper 509 will continually grow.

FIG. 5D shows the plated copper forming on the gold surface of the thin film 503 of the terminal pads to provide electrical contacts to the terminal pads and initiate plating copper thereon. These electroplated joints 510 will then provide an effective means for electrical and mechanical connections between the input/output terminals and the top surface of the dielectric circuitry. The insulating layer 506 has been stripped off.

FIG. 5E shows a plurality of copper circuitry traces 511 formed on the surface of the substrate by conventional etching techniques. These traces 511 extend from a plurality of electroplated copper via holes 507 of the dielectric substrate 504 and serve as electrically connecting channels with respective input/output terminal pads 502 to the external circuitry.

EXAMPLE 4

FIGS. 6A through 6D illustrate a process for producing another embodiment of the flip chip assembly according to the present invention. Referring now to FIG 6A, an integrated circuit chip 601 in which various types of transistor, wiring and the like were formed (not shown) having a plurality of input/output terminal pads 602 exposed. These pads 602 were firstly cleaned by dipping the integrated circuitry chip 601 in a phosphoric

acid solution at room temperature with an immersion time of 10 minutes to remove the surface oxide film. This chip was next dipped in a diluted catalytic solution Enthone "Alumon EN" (trademark) at 25 degree C for 20 seconds to form an thin zinc film 603 on the surface of aluminum alloy terminal pads 602 followed by a thorough distillated water rinse to ensure there is no residue left on the surface of integrated circuitry chip. The integrated circuitry chip was then immersed in a Shipley "NIPOSIT 468" (trademark) electroless plating bath for 2 minutes at 65 degree C. A thin layer of nickel film 604 containing phosphorous was deposited on and around the terminals 602.

FIG. 6B shows a double-sided or multi-layer dielectric substrate 605 having a plurality of copper circuitry traces 606. The traces 606 on one surface of the substrate extend to a plurality of via holes 608 which are pre-metallized with gold plated copper film 607 on the sidewall. These holes 608 are arranged in such a manner that the terminal pads 602 of the integrated circuit chip 601 can be totally or partially exposed when integrated circuit chip 601 is mounted on the substrate 604. These holes 608 are to serve as electrically connecting channels for respective traces 606 on the top surface of the substrate 605 with respective input/output terminal pads 602 of the integrated circuit chips 601.

FIG. 6C shows the integrated circuit chip 601 securely attached to the substrate 605. Tin-lead solder balls 609 are placed into these via holes 608 by a conventional ball placement machine. Enough solder balls 609 should be placed to fill the via holes without exceeding the total volume.

As shown in FIG. 6D, heat is applied to the assembly. When temperature has reached 350 degree C for 1 minute, the solder balls are melted and fill the lower part of the via holes. When the heat is removed, this solder column 610 adheres to the sidewall of the via hole as well as the input/output terminal pads 602 of the integrated circuit chip 601 thus providing an effective means for electrical and mechanical contacts.

CLAIMS

I claim:

1. An integrated circuits assembly, comprising:

(a) a dielectric substrate having a plurality of via holes and electrically conductive material is deposited on sidewall of said via holes;

(b) the said dielectric substrate having a first and second opposite surfaces and a plurality of electrically conductive traces being formed on the first surface of the dielectric substrate, each one of the said traces are extended and connected to the specific said via hole;

(c) an integrated circuit chip having a first surface and a plurality of input/output terminal pads thereon;

(d) the materials on sidewall of said via holes and input/output terminal pad of the said integrated circuit chip are activated for readily initiate electroless plating

(e) means for attaching the said integrated circuit chip to the said dielectric substrate in the orientation of the said via holes in the dielectric substrate are aligned on the top of said terminal pads of the said integrated circuit chip so that the said terminal pads can be totally or partially exposed through the said via holes to the said first surface of the substrate;

(f) electroless plating is applied on the said terminal pads of the said integrated circuit chip as well as the sidewall of the said via holes simultaneously;

(g) the electrolessly plated parts would join together thus provide electrical connections between the said integrated circuit chip and at least one of the first traces on the substrate.

2. The integrated circuit assembly according to claim 1, wherein dielectric material of said substrate is made of plastics.

3. The integrated circuit assembly according to claim 1, wherein dielectric material of said substrate is made of ceramics.

4. The integrated circuit assembly according to claim 1, wherein the said dielectric substrate is a flexible film.

5. The integrated circuit assembly according to claim 1, wherein the said via holes are formed by laser drilling.

6. The integrated circuit assembly according to claim 1, wherein the said via holes are formed by mechanical punching.

7. The integrated circuit assembly according to claim 1, wherein the said via holes are formed by plasma etching.

8. The integrated circuit assembly according to claim 1, wherein the said electrically conductive material on sidewall of said via holes comprises copper.

9. The integrated circuit assembly according to claim 1, wherein the said electrically conductive material on sidewall of said via holes comprises nickel.

10. The integrated circuit assembly according to claim 1, wherein the said electrically conductive material on sidewall of said via holes comprises palladium.

11. The integrated circuit assembly according to claim 1, wherein the said electrically conductive material on sidewall of said via holes comprises gold.

12. The integrated circuit assembly according to claim 8, wherein the said activation method of sidewall of said via holes is by dipping in the palladium containing solution.

13. The integrated circuit assembly according to claim 1, wherein the activation method of input/output terminal pads of said integrated circuit chip is by dipping in the zinc containing solution.

14. The integrated circuit assembly according to claim 1, wherein the activation method of input/output terminal pads of said integrated circuit chip is by dipping in the palladium containing solution.

15. The integrated circuit assembly according to claim 1, wherein the attachment of said integrated circuit chip to the said dielectric substrate is by adhesive film.

16. The integrated circuit assembly according to claim 1, wherein the attachment of said integrated circuit chip to the said dielectric substrate is by liquid adhesives.

17. The integrated circuit assembly according to claim 1, wherein the attachment of said integrated circuit chip to the said dielectric substrate is by mechanical clamping.

18. The integrated circuit assembly according to claim 1, wherein the electroless plating is nickel plating.

19. The integrated circuit assembly according to claim 1, wherein the electroless plating is gold plating.

20. The integrated circuit assembly according to claim 1, wherein the electroless plating is palladium plating.

21. The integrated circuit assembly according to claim 1, wherein the electroless plating is copper plating.

22. A method of forming an integrated circuit assembly comprising the steps of:

(a) a double-sided or multilayer dielectric substrate having a layer of metal film on the first surface of the substrate, and an electrically insulating film being formed on the said metal film;

(b) a plurality of via holes formed in the said dielectric substrate;

(c) an integrated circuit chip having a first surface and a plurality of input/output terminal pads thereon;

(d) depositing a stack of metal film onto the said terminal pads of the said integrated circuit chip to serve as the barrier layer;

(e) attaching the said integrated circuit chip to the said dielectric substrate in the orientation of the said via holes in the dielectric substrate are aligned on the top of said terminals pads so that these said pads can be totally or partially exposed through the said via holes to the said first surface of the substrate;

(f) Activating the said barrier layer and deposit electrically conductive material on the said terminal pads by electroless plating and fill the via holes of said dielectric substrate until reach the said metal layer on the first surface of the substrate and form the connection;

(g) forming a series of electrically conductive traces on said first surface; and interconnect the integrated circuit chip to said first traces by each said filled via holes.

23. The integrated circuit assembly according to claim 22, wherein the said metal film is copper.

24. The integrated circuit assembly according to claim 22, wherein the said a stack of metal film is deposited by sputtering.

25. The integrated circuit assembly according to claim 22, wherein the said a stack of metal film is deposited by evaporation.

26. The integrated circuit assembly according to claim 22, wherein the said a stack of metal film is deposited by electroless plating.

27. A method of forming an integrated circuit assembly comprising the steps of:

(a) a double-side or multilayer dielectric substrate having a layer of metal film on the first surface of the substrate, and an electrically insulating film being formed on the said metal film;

(b) a plurality of via holes with metallized sidewall being formed in the said dielectric substrate;

(c) an integrated circuit chip having a first surface and a plurality of input/output terminal pads thereon

(d) depositing a stack of metal film onto the said terminal pads of the said integrated circuit chip to serve as the barrier and conductive layer

(e) attaching the said integrated circuit chip to the said dielectric substrate in the orientation of the said via holes in the dielectric substrate

are aligned on the top of said terminal pads of the said integrated circuit chip so that these said pads can be totally or partially exposed through the said via holes to the said first surface of the substrate;

(f) deposit electrically conductive material on the sidewall of the said via holes by electrochemical plating, extending the said metallized sidewall of said dielectric substrate, until contact and initiate the plating on the surface of the said terminal pads and form the connections;

(g) forming a series of electrically conductive traces on said first surface; and interconnect the integrated circuit chip to said traces through each said via hole.

28. The integrated circuit assembly according to claim 27, wherein the said electrochemical plating is copper plating

29. The integrated circuit assembly according to claim 27, wherein the said electrochemical plating is gold plating.

30. The integrated circuit assembly according to claim 27, wherein the said electrochemical plating is nickel plating.

31. An integrated circuit assembly, comprising:

(a) a dielectric substrate having a first and second opposite surfaces and a plurality of electrically conductive traces being formed on the first surface of the dielectric substrate;

(b) a plurality of via holes formed in the dielectric substrate, each via hole extending to one of the said traces and depositing electrically conductive material on sidewall of said via holes to electrical contact with selected ones of said first traces;

(c) an integrated circuit chip having a first surface and a plurality of input/output terminal pads thereon;

(d) means for attaching the said integrated circuit chip to the said dielectric substrate in the orientation of the said via holes in the dielectric substrate are aligned on the top of said terminal pads of the said integrated circuit chip so that these said pads can be totally or partially exposed through the said via holes to the said first surface of the substrate;

(f) means for placing electrically conductive material in the said via holes and on the said input/output terminal pads;

(g) energy source is applied to enhance the contact of the said conductive material to the said sidewall of the via holes and the terminal pads of the said chip thus providing electrical contacts between the said integrated circuit chip and at least one of the first traces on the said substrate.

32. The integrated circuit assembly according to claim 31, wherein said placement means is by printing.

33. The integrated circuit assembly according to claim 32, wherein said conductive material is solder paste.

34. The integrated circuit assembly according to claim 31, wherein the said placement means is by jetting.

35. The integrated circuit assembly according to claim 34, wherein the said conductive material is liquid solder.

36. The integrated circuit assembly according to claim 31, wherein the said placement means is by mechanical placement.

37. The integrated circuit assembly according to claim 36, wherein the said conductive material is solder particle.

38. The integrated circuit assembly according to claim 31, wherein the said conductive material is epoxy adhesives.

39. The integrated circuit assembly according to claim 31, wherein the said conductive material is intrinsic conductive polymer.

40. The integrated circuit assembly according to claim 31, wherein the said energy source is laser.

41. The integrated circuit assembly according to claim 31, wherein the said energy source is heat.

42. The integrated circuit assembly according to claim 31, wherein the said energy source is infrared.

FIG. 1

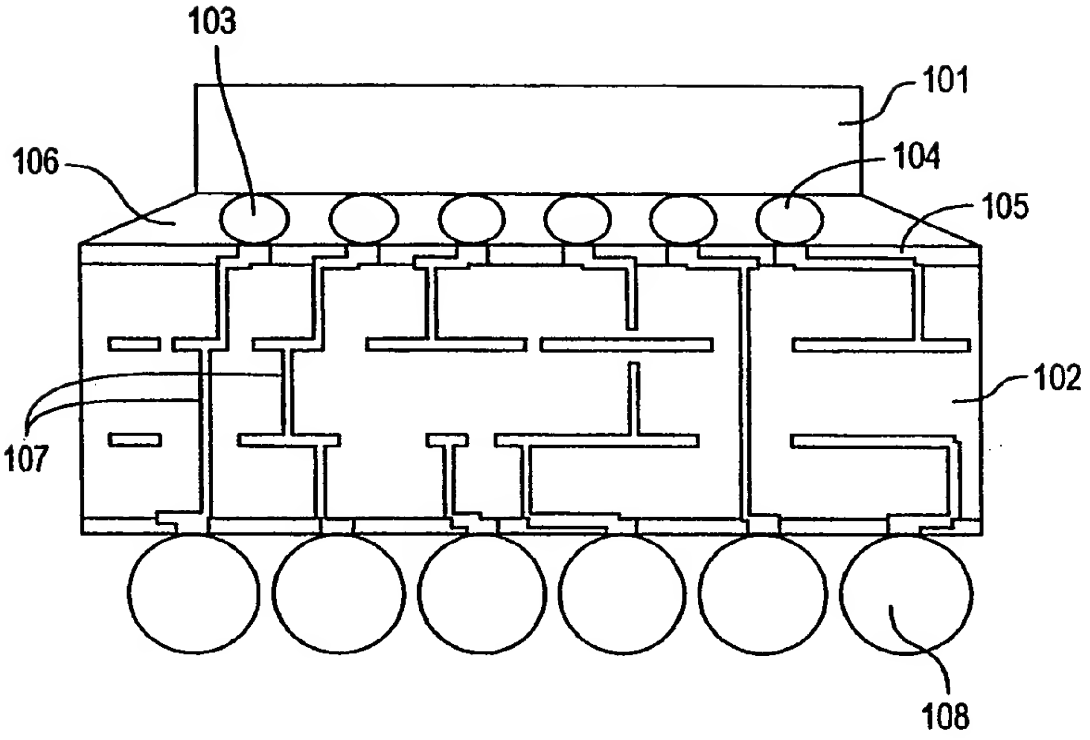


FIG. 2

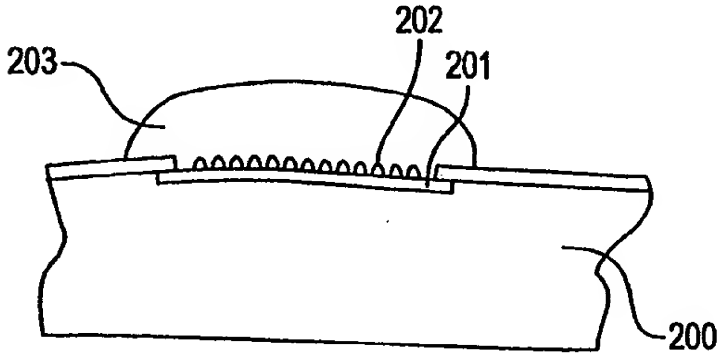


FIG. 3A

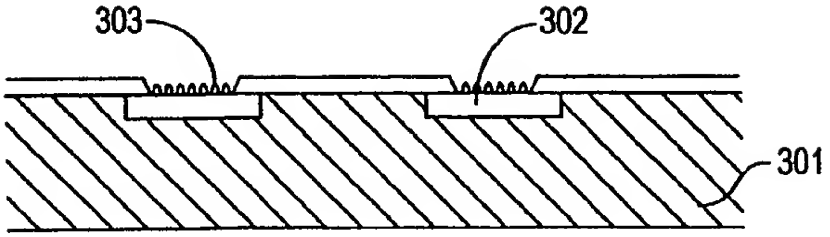


FIG. 3B

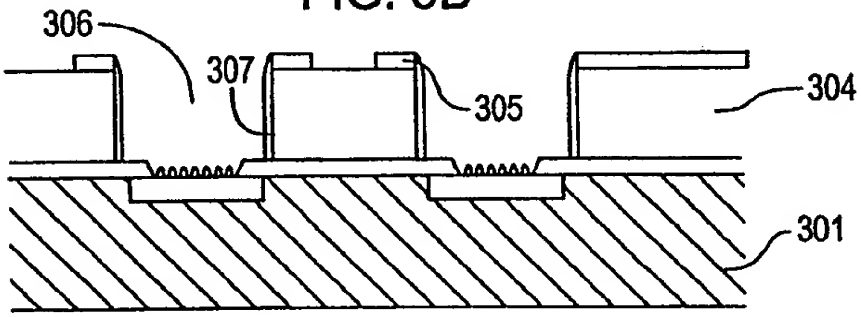


FIG. 3C

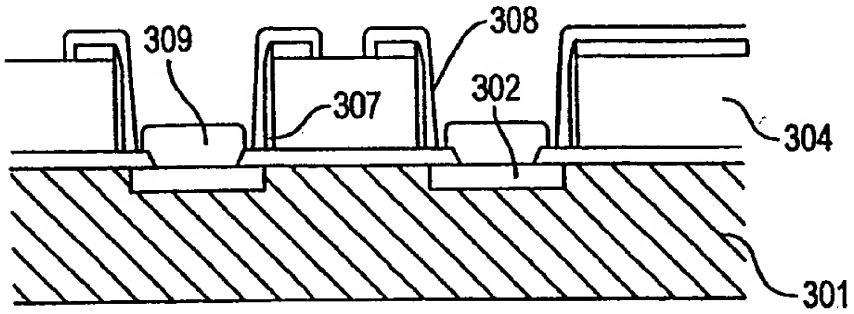


FIG. 3D

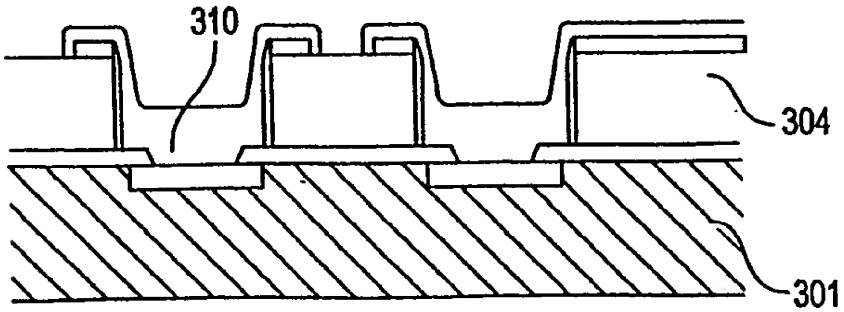


FIG. 4A

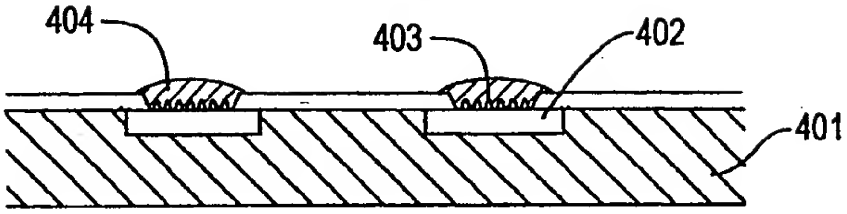


FIG. 4B

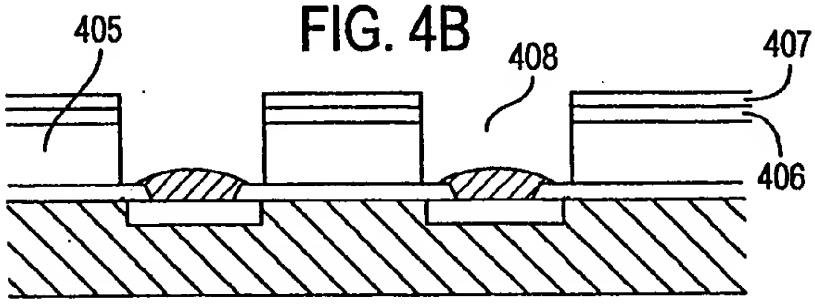


FIG. 4C

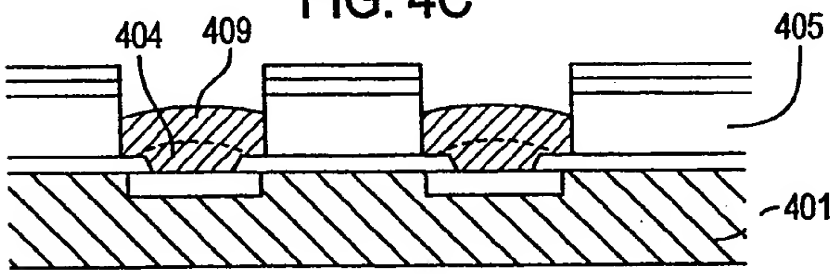


FIG. 4D

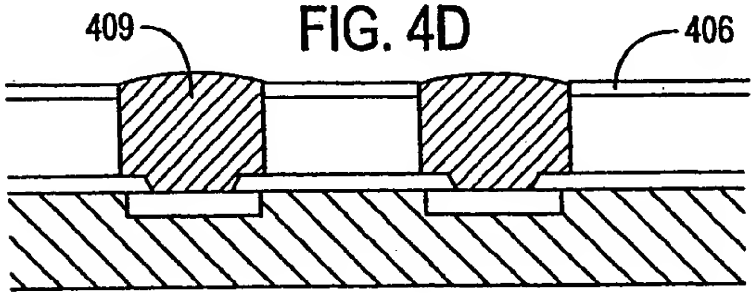


FIG. 4E

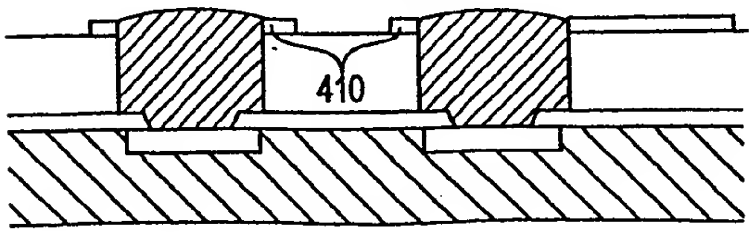


FIG. 5A

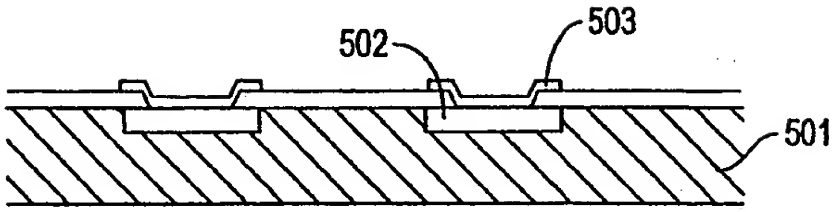


FIG. 5B

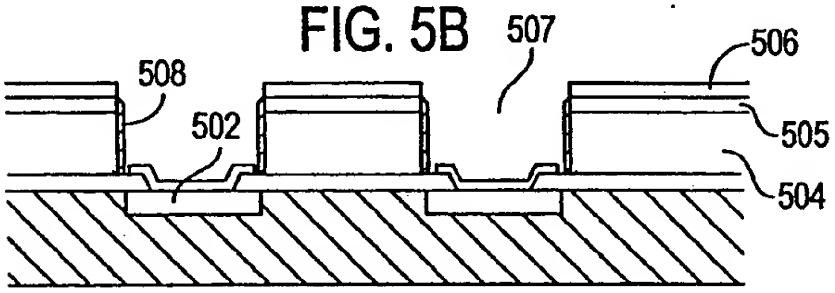


FIG. 5C

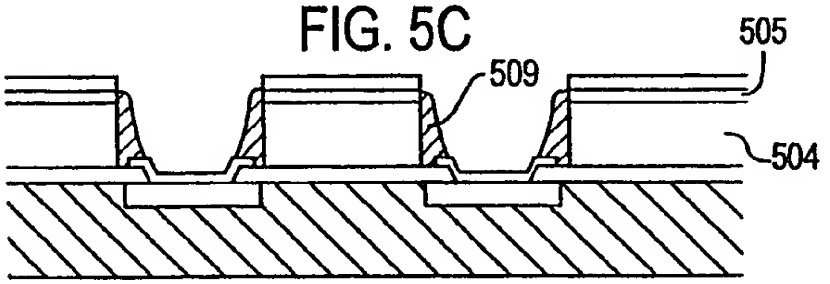


FIG. 5D

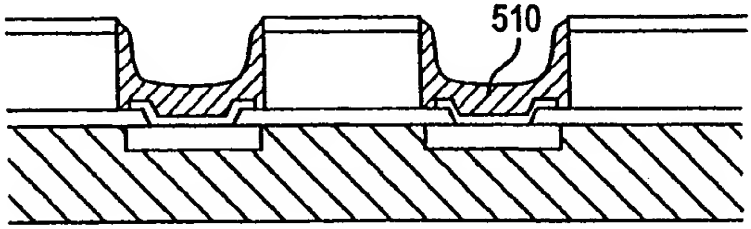


FIG. 5E

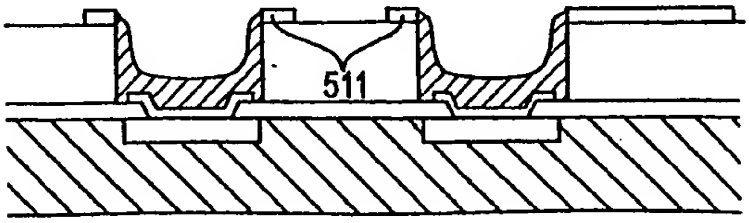


FIG. 6A

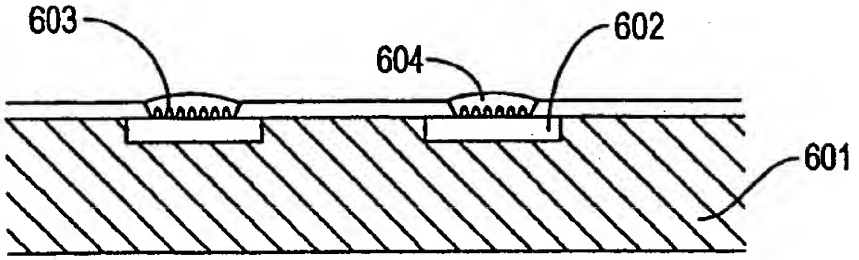


FIG. 6B

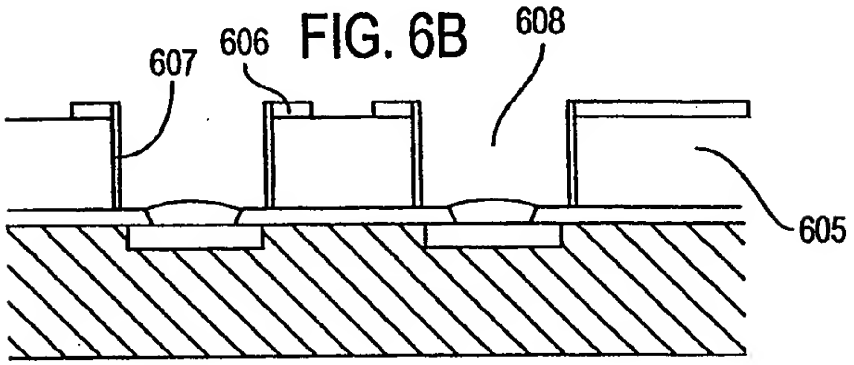


FIG. 6C

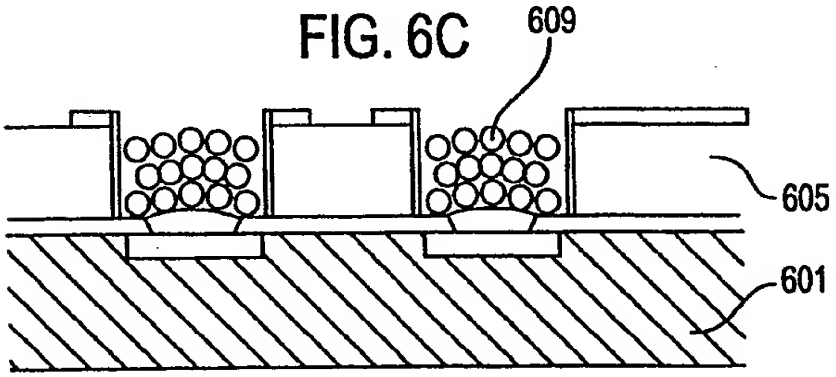
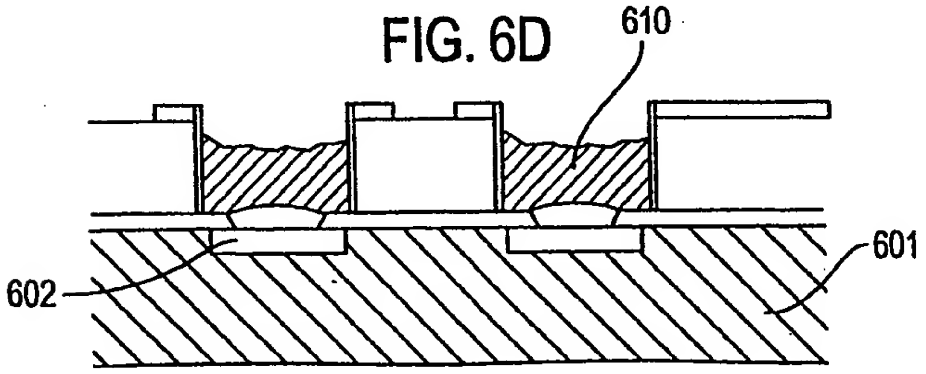


FIG. 6D



INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG 99/00035

A. CLASSIFICATION OF SUBJECT MATTER

IPC[6]: H 01 L 23/48, 21/44

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC[6]: H 01 L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI, EPODOC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 355 283 A (MARSS et al.), 11 October 1994 (11.10.94), totality, especially claims.	1,22,27,31
A	WO 97/38 563 A1 (PROLINX LABS CORPORATION), 16 October 1997 (16.10.97), fig.; claims.	1,22,27,31
A	US 5 106 461 A (VOLFSON et al.), 21 April 1992 (21.04.92), claim 1; fig.	1,22,27,31
A	EP 0 718 882 A1 (ADVANCED SEMICONDUCTOR ASSEMBLY TECHNOLOGY, INC.), 26 June 1996 (26.06.96).	

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
„A" document defining the general state of the art which is not considered to be of particular relevance
„E" earlier application or patent but published on or after the international filing date
„L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
„O" document referring to an oral disclosure, use, exhibition or other means
„P" document published prior to the international filing date but later than the priority date claimed
„T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
„X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
„Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
„&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 September 1999 (17.09.99)	28 September 1999 (28.09.99)
Name and mailing adress of the ISA/AT Austrian Patent Office Kohlmarkt 8-10; A-1014 Vienna Facsimile No. 1/53424/200	Authorized officer Heinich Telephone No. 1/53424/454

Form PCT/ISA/210 (second sheet) (July 1998)

In Recherchenbericht angeführtes Patentdokument Patent document cited in search report Document de brevet cité dans le rapport de recherche	Datum der Veröffentlichung Publication date Date de publication	Mitglied(er) der Patentfamilie Patent family member(s) Membre(s) de la famille de brevets	Datum der Veröffentlichung Publication date Date de publication
US A 5355283	11-10-1994	JP A2 7074281	17-03-1995
WO A1 9738563	16-10-1997	AU A1 24335/97 US A 5872338	29-10-1997 16-02-1999
US A 5106461	21-04-1992	EP A1 425607 JP T2 3505270 US A 4980034 WO A1 9012483	08-05-1991 14-11-1991 25-12-1990 18-10-1990
EP A1 718882	26-06-1996	US A 5397921 US A 5409865	14-03-1995 25-04-1995